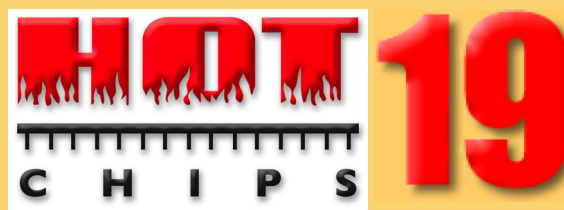


# Conference Day 1

## Monday, August 20



9:00 - 9:15am **Opening Remarks**

9:15 - 10:45 **Session One** **IBM POWER6™**

<b>Fault-Tolerant Design of the IBM POWER6™ Microprocessor</b>	IBM
<b>System Performance Scaling of IBM POWER6™ Based Servers</b>	IBM
<b>The Third Generation of IBM's Elastic Interface on POWER6™</b>	IBM

11:15 - 12:15 **Keynote** **Digital Gaia**

**Vernor Vinge** Computer Scientist, Science Fiction Writer, author of *True Names* and *Rainbows End*

12:15 - 1:15 **Lunch**

1:15 - 2:45 **Session Two** **Multi-Core and Parallelism I**

<b>NVIDIA GeForce 8800™ GPU</b>	NVIDIA
<b>The NVIDIA GPU Parallel Computing Architecture &amp; CUDA Programming Model</b>	NVIDIA
<b>Performance Insights of Executing Non-Graphics Applications on the NVIDIA GeForce 8800™ &amp; the CUDA™ Parallel Programming Environment</b>	NVIDIA, UIUC

3:15 - 5:15 **Session Three** **Multi-Core and Parallelism II**

<b>AMD's Radeon™ HD 2900 - 2<sup>nd</sup> Generation Unified Shader Architecture</b>	AMD
<b>Teraflops Prototype Processor with 80 Cores</b>	Intel
<b>TRIPS: A Distributed Explicit Data Graph Execution (EDGE) Microprocessor</b>	UT - Austin
<b>The Tile Processor™ Architecture: Embedded Multicore for Networking and Digital Multimedia</b>	Tilera

5:45 - 7:15 **Session Four** **Embedded and Video**

<b>SH-X3: Flexible SuperH Multi-Core for High-Performance and Low-Power Embedded System</b>	Renasas, Hitachi
<b>An Innovative HD Video and Digital Image Processor for Low-Cost Digital Entertainment Products</b>	Texas Instruments
<b>Professional H.264/AVC CODEC Chip-Set for High-Quality HDTV Broadcast Infrastructure and High-End Flexible CODEC Systems</b>	NTT Cyber Space Labs

7:15 - 8:15 **Dinner**

8:15 - 9:45 **Panel Discusson** **What's next beyond CMOS?**

Moderator: Norm Jouppi	HP Labs
Panelists: Mark Horowitz	Stanford University,
John Kubiatowicz	UC Berkeley,
Mike Mayberry	Intel,
Ghavam Shahidi	IBM,
Stan Williams	Hewlett-Packard



Conference Day 2  
Tuesday, August 21

8:00-9:30	<b>Session Five</b>	<b>Technology and Software Directions</b>
	Multiterabit Switch Fabrics Enabled by Proximity Communication Thyristor RAM (T-RAM) - A High-Speed High-Density Embedded Memory Technology for Nano-Scale CMOS Raksha: A Flexible Architecture for Software Security	Sun Microsystems Labs T-RAM Semiconductor  Stanford University
9:30-10:30	<b>Session Six</b>	<b>Wireless</b>
	A 2x2 MIMO Baseband for High-Throughput Wireless Local-Area Networking (802.11n) A 4 Gbps Wireless True Uncompressed 1080p-Capable HD A/V Transceiver using 60 GHz	Broadcom  SiBeam
10:30-11:00		
11:00-12:00	<b>Keynote</b>	
	<b>Multicore and Beyond: Evolving the x86 Architecture</b> Phil Hester, Chief Technology Officer, AMD	
12:00 - 1:00	<b>Lunch</b>	
1:00 - 1:30	<b>Special Presentation</b>	
	<b>Wireless Broadband and Entrepreneurship in America</b> Reed Hundt, Vice-Chairman, Frontline Wireless, Former Chair, FCC	
1:30-3:00	<b>Session Seven</b>	<b>Networking</b>
	Chesapeake: A 50 Gbps Network Processor and Traffic Manager Tolapai - A System on a Chip with Integrated Accelerators Fulcrum's FocalPoint II - A 300ns, 240Gb/s Switch/Router	Bay Microsystems Intel Fulcrum Microsystems
3:20-4:50	<b>Session Eight</b>	<b>Mobile PC Processors and Chipsets</b>
	Advanced Power Management Features in Penryn: 45nm Next Generation Intel Core™ 2 Duo Next Generation Mobile X86 Processor from AMD nForce 680i and 680a, NVIDIA's Next Generation Platform	Intel Fulcrum Microsystems AMD NVIDIA
4:50-5:10		
5:10-6:10	<b>Session Nine</b>	<b>Big Iron</b>
	VictoriaFalls - Scaling Highly-Threaded Processor Cores The Next Generation Mainframe Microprocessor	Sun Microsystems IBM
6:10-6:15	<b>Closing Remarks</b>	